

PTO/SB/08A (10-96)

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	Substitute	01 10HH 1448AVP10	Application Number	10/045,055	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	January 15, 2002
				First Named Inventor	Benoudiz
	SIAIDN	IENI DI AIILI	Group Art Unit	2133	
	(use as	s many sheets as necessa	ry)	Examiner Name	
Sheet	1	of	1	Attorney Docket Number	24773
	1				Previously V02/16

			U.S. PATENT DOCUMENTS		
	Cite No.	U.S. Patent Document		Date of Publication of Cited Document MM-DD-YYYY	Pages, columns, lines, Where Relevant Passages or Relevant Figures Appear
Examiners Initials		Nurnber Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document		
CK	AA	4,937,765	Shupe et al	06-26-1990	
OW	AB	5,202,889	Aharon et al	04-13-1993	
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		OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS	
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
·QC	AG	Benjamin et al, A Study in Coverage-Driven Test Generation, DAC, 1999, pp. 970 – 975	
<i>مح</i>	AH	Debany Jr. et al, Design Verification Using Logic Tests, IEEE, 1992, pp. 17 – 24	
ck	AI	Moundanos, et al., Abstraction Techniques for Validation Coverage Analysis and Test Generation, IEEE Transactions on Computers, Vol. 47, No. 1, January 1998, pp. 2 – 14	· · · · · · · · · · · · · · · · · · ·
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de	AK	Greggain et al, Fault Grading, A Measure of Logic Simulation Integrity, Proc. 2 nd Annual IEEE ASIC Seminar and Exhibit, 1989, pp 9-2.1 – 9-2.4	· -
CK	AL	Sneed, State Coverage of Embedded Realtime Programs, Proc. 2 nd Workshop on Software Testing, Verification & Analysis, 1988, pp 245	

Examiner Signature Chuke	Serd sel	Date Considered	2113/06
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